IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A duty cycle correction circuit comprising:

a delay unit for receiving a first clock signal in which a first logic value has a shorter period of time per cycle than a second logic value, delaying the first clock signal, and outputting a second clock signal which transitions to the second logic value at a timing at which the period of time equivalent to a half cycle has elapsed since the first clock signal transitioned to the first logic value; and

a clock-signal output unit for outputting a third clock signal based on the first and second clock signals,

wherein the clock-signal output unit comprises: a first output unit for setting the third clock signal at a first logic output value with either one of the first logic value and the second logic value in response to the transition of the first clock signal to the first logic value; and a second output unit for setting the third clock signal at a second logic output value with the other of the first logic value and the second logic value in response to the transition of the second clock signal to the second logic value,

the delay unit includes a transfer gate which is put into condition to pass the first clock signal to output the second clock signal,

the transfer gate includes a transistor whose gate and drain are connected to each other, and

the duty cycle correction circuit receives the first clock signal and corrects the duty cycle of the first clock ~~received~~ signal to output the third clock signal.

2. (Currently amended) A 50% duty cycle clock-signal production circuit comprising:

a delay unit for receiving a first clock signal in which a first logic value has a shorter period of time per cycle than a second logic value, delaying the first clock signal and outputting a second clock signal which transitions to the second logic value at a timing at which the period of time equivalent to a half cycle has elapsed since the first clock signal transitioned to the first logic value;

a clock-signal output unit for outputting a third clock signal based on the first and second clock signals; and ~~The circuit of claim 1, wherein~~

~~the first clock signal is produced by~~ a frequency divider circuit for producing the first clock signal,

wherein the clock-signal output unit comprises:

a first output unit for setting the third clock signal at a first logic output value with either one of the first logic value and the second logic value in response to the transition of the first clock signal to the first logic value; and

a second output unit for setting the third clock signal at a second logic output value with the other of the first logic value and the second logic value in response to the transition of the second clock signal to the second logic value.

3. (Currently amended) The circuit of claim 2 [[1]],

wherein the first output unit includes a first transistor which is of either one of n-channel type and p-channel type and whose gate receives the first clock signal,

the second output unit includes a second transistor which is of the other of n-channel type and p-channel type, whose gate receives the second clock signal and whose drain is connected to a drain of the first transistor, and

the third clock signal is based on a signal output from the common drain of the first and

second transistors.

4-5. (Cancelled)

6. (Currently amended) The circuit of claim 1 [[5]],

wherein the first clock signal is produced by a frequency divider ~~clock-signal production~~ circuit formed of at least one n-channel transistor and at least one p-channel transistor,

the clock-signal output unit is formed of at least one n-channel transistor and at least one p-channel transistor, and

~~the transistor forming the delay unit has either one of the n- and p-channel types in respect of which type transistors included in the clock-signal production circuit and in the first output unit of the clock-signal output circuit and tuned on when the third clock signal transitions to the first logic output value are different in number from transistors included in the clock-signal production circuit and in the second output unit of the clock-signal output circuit and turned on when the third clock signal transitions to the second logic output value~~

the numbers of n-channel and p-channel transistors through which a signal travels in the rising of the third clock signal are equal to those through which a signal travels in the falling of the third clock signal.

7. (Currently amended) The circuit of claim 2 [[1]], wherein the delay unit includes a transistor whose gate is supplied with a predetermined voltage and of which either one of a source and a drain receives the first clock signal to output the second clock signal from the other of the drain and the source, and

the predetermined voltage supplied to the gate of the transistor is above a gate threshold value in the case where the transistor is an n-channel transistor while the predetermined voltage supplied to the gate of the transistor is below the gate threshold value in the case where the

transistor is a p-channel transistor.

8. (Currently amended) The circuit of claim 7, wherein the frequency divider ~~first clock signal is produced by a clock-signal production~~ circuit is formed of at least one n-channel transistor and at least one p-channel transistor,

the clock-signal output unit is formed of at least one n-channel transistor and at least one p-channel transistor, and

~~the transistor forming the delay unit has either one of the n- and p-channel types in respect of which type transistors included in the clock-signal production circuit and in the first output unit of the clock-signal output circuit and tuned on when the third clock signal transitions to the first logic output value are different in number from transistors included in the clock-signal production circuit and in the second output unit of the clock-signal output circuit and turned on when the third clock signal transitions to the second logic output value~~

the numbers of n-channel and p-channel transistors through which a signal travels in the rising of the third clock signal are equal to those through which a signal travels in the falling of the third clock signal.